Amendment of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (Currently Amended) The DC/DC converter described in Claim[1] 6 wherein the first capacitor is a one capacitor element.

3. (Previously Presented) The DC/DC converter described in Claim 2 wherein the capacitance of the first capacitor is approximately equal to that of the second capacitor.

4. (Currently Amended) The DC/DC converter described in [any of] Claim [1] 6 wherein the duty ratios of the first and second phases are set at about ½.

5. (Currently Amended) A charge pump type DC/DC converter comprising:

a voltage input terminal connected to the output terminal of a DC power supply;

first and second capacitors;

a voltage output terminal connected to a load;

a switch circuit network having a first phase, in which a first terminal of the first capacitor is connected to the voltage input terminal, a first terminal of the second capacitor is connected to the voltage output terminal, and a second terminal of the first capacitor and a second terminal of the second capacitor are connected to each other, and a second phase, in which the first and second terminals of the first capacitor are connected to the voltage output terminal and the voltage input terminal, respectively, and the first and second terminals of the second capacitor are connected to the voltage input terminal and a reference potential, respectively;

a switching controller that controls the switch circuit network to switch the first and second phases alternately at prescribed duty ratios;

[The DC/DC converter described in Claim 1 wherein]

the switch circuit network comprises:

a first MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the first capacitor;

a second MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the first capacitor;

a third MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the second capacitor;

a fourth MOS transistor with a first terminal connected to the second terminal of the first capacitor and a second terminal connected to the second terminal of the second capacitor;

a fifth MOS transistor with a first terminal connected to the second terminal of the second capacitor and a second terminal connected to the reference potential;

a sixth MOS transistor with a first terminal connected to the first terminal of the first capacitor and a second terminal connected to the voltage output terminal; and

a seventh MOS transistor with a first terminal connected to the first terminal of the second capacitor and a second terminal connected to the voltage output terminal;

in the first phase, the switching controller keeps the first, fourth, and seventh MOS transistors in the on state, and the second, third, fifth, and sixth MOS transistors in the off state; and wherein

in the second phase, the switching controller keeps the first, fourth, and seventh MOS transistors are kept in the off state, and the second, third, fifth, and sixth MOS transistors in the on state.

6. (Currently Amended) A charge pump type DC/DC converter comprising:

a voltage input terminal connected to the output terminal of a DC power supply;

first and second capacitors;

a voltage output terminal connected to a load;

a switch circuit network having a first phase, in which a first terminal of the first capacitor is connected to the voltage input terminal, a first terminal of the second capacitor is connected to the voltage output terminal, and a second terminal of the first capacitor and a second terminal of the second capacitor are connected to each other, and a second phase, in which the first and second terminals of the first capacitor are connected to the voltage output terminal and the voltage input terminal, respectively, and the first and second terminals of the second capacitor are connected to the voltage input terminal and a reference potential, respectively;

a switching controller that controls the switch circuit network to switch the first and second phases alternately at prescribed duty ratios;

[The DC/DC converter described in Claim 1] wherein the first capacitor is comprised of n (n is an integer of 2 or larger) capacitor elements, the n capacitor elements are connected in series in the first phase, and the n capacitor elements are connected in parallel with each other in the second phase, and wherein output voltage (V_{olt} is defined by $V_{olt} = [1+1/(N+1)].Vinput$

7. (Previously Presented) The DC/DC converter described in Claim 6 wherein the n capacitor elements have approximately the same capacitance.

8. (Previously Presented) The DC/DC converter described in Claim 6 wherein the duty ratio of the first phase is set at about 1/(n+1), and the duty ratio of the second phase is set at about n/(n+1).

9. (Previously Presented) The DC/DC converter described in Claim 6 wherein the first capacitor is comprised of first and second capacitor elements and the switch circuit network comprises:

a first MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the first capacitor element;

a second MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the first capacitor element;

a third MOS transistor with a first terminal connected to the second terminal of the first capacitor element and a second terminal connected to the first terminal of the second capacitor element;

a fourth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the second capacitor element;

a fifth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the second capacitor;

a sixth MOS transistor with a first terminal connected to the second terminal of the second capacitor element and a second terminal connected to the second terminal of the second capacitor;

a seventh MOS transistor with a first terminal connected to the second terminal of the second capacitor and a second terminal connected to the reference potential;

an eighth MOS transistor with a first terminal connected to the first terminal of the first capacitor element and a second terminal connected to the voltage output terminal;

a ninth MOS with a first terminal connected to the first terminal of the second capacitor element and a second terminal connected to the voltage output terminal; and

a tenth MOS transistor with a first terminal connected to the first terminal of the second capacitor and a second terminal connected to the voltage output terminal;

in the first phase, the switching controller keeps the first, third, sixth, and tenth MOS transistors in the on state, and the second, fourth, fifth, seventh, eighth, and ninth MOS transistors in the off state;

wherein in the second phase, the switching controller keeps, the first, third, sixth, and tenth MOS transistors in the off state, and the second, fourth, fifth, seventh, eighth, and ninth MOS transistors in the on state.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Currently Amended) The DC/DC converter described Claim [10] 6 wherein the first capacitor is comprised of first and second capacitor elements; the switch circuit network has the following:

a first MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the first capacitor element;

a second MOS transistor with a first terminal connected to the second terminal of the first MOS transistor and a second terminal connected to the first terminal of the second capacitor element;

a third MOS transistor with a first terminal connected to the second terminal of the first capacitor element and a second terminal connected to the first terminal of the second capacitor element;

a fourth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the second capacitor element;

a fifth MOS transistor with a first terminal connected to the second terminal of the first capacitor element and a second terminal connected to the second terminal of the second capacitor element;

a sixth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the second capacitor;

a seventh MOS transistor with a first terminal connected to the second terminal of the second capacitor element and a second terminal connected to the second terminal of the second capacitor;

an eighth MOS transistor with a first terminal connected to the second terminal of the second capacitor and a second terminal connected to the reference potential;

a ninth MOS transistor with a first terminal connected to the first terminal of the first capacitor element and a second terminal connected to the voltage output terminal; and

a tenth MOS transistor with a first terminal connected to the first terminal of the second capacitor and a second terminal connected to the voltage output terminal;

in the first phase, the switching controller keeps the first, second, fifth, seventh, and tenth MOS transistors in the on state, and the third, fourth, sixth, eighth, and ninth MOS transistors in the off state; and wherein

in the second phase, the switching controller keeps the first, second, fifth, seventh, and tenth MOS transistors in the off state, and the third, fourth, sixth, eighth, and ninth MOS transistors in the on state.

14. (Currently Amended) The DC/DC converter described in Claim [1] 6 the first capacitor is comprised of n x m (n and m are integers of 2 or larger) capacitor elements; in the first phase, for the nxm capacitor elements, all n capacitor elements are connected in series, and these serial capacitor circuits are connected in parallel in

m columns; in the second phase, for the n x m capacitor elements, all m capacitor elements are connected in series, and these serial capacitor circuits are connected in parallel in n columns.

15. (Previously Presented) The DC/DC converter described in Claim 14 wherein the n x m capacitors have approximately the same capacitance.

16. (Previously Presented) The DC/DC converter described in Claim 14 wherein the duty ratio of the first phase is set at about m/(n+m), and the duty ratio of the second phase is set at about n/(n+m).

17. (Previously Presented) The DC/DC converter described in Claim 14 wherein the first capacitor is comprised of first, second, third, and fourth capacitor elements; the switch circuit network comprises:

a first MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the third capacitor element;

a second MOS transistor with a first terminal connected to the first terminal of the third capacitor element and a second terminal connected to the first terminal of the first capacitor element;

a third MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the first capacitor element;

a fourth MOS transistor with a first terminal connected to the second terminal of the first capacitor element and a second terminal connected to the first terminal of the second capacitor element;

a fifth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the second capacitor element;

a sixth MOS transistor with a first terminal connected to the second terminal of the third capacitor element and a second terminal connected to the first terminal of the fourth capacitor element;

a seventh MOS transistor with a first terminal connected to the first terminal of the first capacitor element and a second terminal connected to the second terminal of the third capacitor element;

an eighth MOS transistor with a first terminal connected to the first terminal of the second capacitor element and a second terminal connected to the second terminal of the fourth capacitor element;

a ninth MOS transistor with a first terminal connected to the second terminal of the second capacitor element and a second terminal connected to the second terminal of the fourth capacitor element;

a tenth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the second capacitor;

an eleventh MOS transistor with a first terminal connected to the second terminal of the fourth capacitor element and a second terminal connected to the second terminal of the second capacitor;

a twelfth MOS transistor with a first terminal connected to the second terminal of the second capacitor and a second terminal connected to the reference potential;

a thirteenth MOS transistor with a first terminal connected to the first terminal of the third capacitor element and a second terminal connected to the voltage output terminal;

a fourteenth MOS transistor with a first terminal connected to the first terminal of the fourth capacitor element and a second terminal connected to the voltage output terminal;

a fifteenth MOS transistor with a first terminal connected to the first terminal of the second capacitor and a second terminal connected to the voltage output terminal;

in the first phase, the switching controller keeps the first, second, fourth, sixth, ninth, eleventh, and fifteenth MOS transistors in the on state, and the third, fifth, seventh, eighth, tenth, twelfth, thirteenth, and fourteenth MOS transistors in the off state;

in the second phase, the switching controller keeps the first, second, fourth, sixth, ninth, eleventh, and fifteenth MOS transistors in the off state, and the third, fifth, seventh, eighth, tenth, twelfth, thirteenth, and fourteenth MOS transistors in the on state.

18. (Currently Amended) The DC/DC converter described in Claim [1] 6 further comprising a third capacitor for smoothing with a first terminal connected to the voltage output terminal and a second terminal connected to the reference potential.

19. (Currently Amended) The DC/DC converter described in Claim [1] 6wherein

a current control circuit that is connected in series between the voltage input terminal and the first capacitor,

a voltage detector is used for detecting the output voltage obtained at the voltage output terminal,

a reference voltage generator that can generates a reference voltage corresponding to the set value of the output voltage output from the voltage output terminal, and

a current controller compares the output voltage detected by the voltage detector with the reference voltage and controls the current in the current control circuit corresponding to the comparison error.

20. (Previously Presented) The DC/DC converter described in Claim 5 wherein all of the MOS transistors are turned off simultaneously in the phase switching period between the first and second phases.